REMARKS

Claims 1-33 were pending before this amendment. In this amendment claims 17-33 and 30-33 are cancelled. Claim 34 is new. Claims 1-11, 13-16, 24-26, 28 and 29 were rejected. Claims 12 and 27 would be allowable if re-written in independent form with all intervening limitations.

Applicant confirms election of Group I, Claims 1-16 and 24-29, with traverse. Claims 17-23 and 30-33 are cancelled without prejudice and Applicant reserves the right to purse them in a continuation or divisional application.

Claims 1-11, 13-16, 24-26, 28 and 29 were rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 6,538,470 (hereinafter referred to as Langhammer). Applicant respectfully traverses the rejections.

Landhammer describes in Fig. 5, column 14, lines 25-38, a programmable logic device with and input/output perimeter ring as represented by input/out interfaces 120. These input/out interfaces 120 are shown at the top of each column of logic array block (LAB) 108. Fig. 9 is a blow-up of area 110, which is part of column 118 in Fig. 1. Area 128 shows the digital signal processing block [col. 18, lines 3-23]. As discloses in the background and Fig. 1 of the specification, Landhammer's perimeter ring as represented by input/out interfaces 120, is similar to the I/O ring 4 of Fig. 1 of the specification.

Claim 1 has been amended to include, among other features, that there does not exist a perimeter input/output (I/O) ring. This is supported by Fig. 3 and paragraphs [0011], and [0027]-[0028], of the specification. Since Langhammer teaches a perimeter I/O ring, claim 1 should now be allowable.

Claims 2-9 being dependent upon claim 1 should be allowable for at least the same reason claim 1 is allowable. In addition, in regards to the rejection of claim 4, Multi-giga bit transceiver (MGT) is a transceiver that processes multiple gigabits (giga is one million or 10^6) per second, not a multiple of bits. Thus the Applicant requests withdrawal of this rejection.

Claim 10 has been amended to include, among other features, wherein when the circuit elements of the first set comprise logic blocks there is no input/output block between the end of the first column and the side of the IC. As shown by Fig. 5 in

Langhammer there is an I/O interface 120 between the end of the logic array blocks 108 and the side of the IC. Hence, claim 10 should now be allowable.

Claims 11-16 being dependent upon claim 10 should be allowable for at least the same reason claim 10 is allowable.

Claim 24 has been amended to include, among other features, wherein when the first circuit type comprises logic blocks and the first column does not have an input/output block at an end of the first column,. As shown by Fig. 5 in Langhammer there is an I/O interface 120 at the end of the logic array blocks 108. Hence, claim 24 should now be allowable.

Claims 25-29 being dependent upon claim 24 should be allowable for at least the same reason claim 24 is allowable.

New claim 34 has been added which incorporates the limitations of claims 10 and 12 and should be allowable for the reasons claim 12 is allowable.
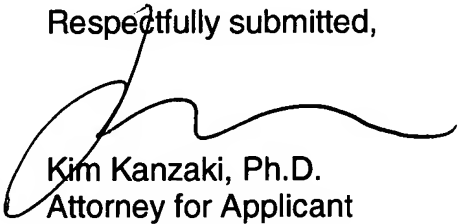
Applicant hereby submits for the examiner's review a Supplemental Information Disclosure Statement citing six (6) references.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.
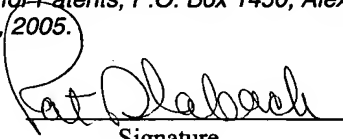
If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on June 24, 2005.

__Pat Slaback__
Name   Signature